International Journal of Computer Science and Engineering (IJCSE)
ISSN (P): 2278–9960; ISSN (E): 2278–9979
Vol. 12, Issue 2, Jul–Dec 2023; 115–140

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

PRE-SILICON VALIDATION TECHNIQUES FOR SOC DESIGNS: A COMPREHENSIVE ANALYSIS

Ashvini Byri[1], Murali Mohana Krishna Dandu[2], Raja Kumar Kolli[3], Dr Satendra Pal Singh[4], Prof.(Dr) Punit Goel[5] & Om Goel[6]

[1]Scholar, University of Southern California, Parel, Mumbai, India

[2]Scholar, Texas Tech University, San Jose, CA

[3]Scholar, Wright State University, CO, 80104, USA,

[4]Independent Researcher, Ex-Dean, Gurukul Kangri University, Haridwar, Uttarakhand, India

[5]Research Supervisor, Maharaja Agrasen Himalayan Garhwal University, Uttarakhand, India

[6]Independent Researcher, ABES Engineering College Ghaziabad, India

ABSTRACT

The increasing complexity of System on Chip (SoC) designs necessitates robust pre-silicon validation techniques to ensure functionality, performance, and reliability before fabrication. This paper presents a comprehensive analysis of pre-silicon validation methodologies, emphasizing their critical role in mitigating risks associated with design flaws. Various techniques, including simulation-based validation, formal verification, and emulation, are explored in detail, highlighting their strengths and limitations.

Simulation-based validation enables exhaustive testing of design behavior under diverse scenarios, while formal verification ensures logical correctness through mathematical proofs, significantly reducing the likelihood of corner-case failures. Emulation, on the other hand, provides a near-real-time environment for validating system performance and integration, allowing for early detection of potential issues. Additionally, this paper discusses the integration of advanced tools and methodologies, such as Assertion-Based Verification (ABV) and coverage-driven verification, which enhance the effectiveness of pre-silicon validation processes.

Furthermore, we examine the impact of emerging technologies, including machine learning and artificial intelligence, on improving validation efficiency and accuracy. The adoption of these innovative approaches is anticipated to revolutionize the pre-silicon validation landscape, paving the way for more reliable and faster SoC designs. In conclusion, this paper aims to provide insights into the evolving practices in pre-silicon validation, offering valuable guidance for researchers and practitioners striving for excellence in SoC design and development.

KEYWORDS: *Pre-Silicon Validation, Soc Design, Simulation-Based Validation, Formal Verification, Emulation, Assertion-Based Verification, Coverage-Driven Verification, Design Reliability, Machine Learning, Artificial Intelligence*

Article History

Received: *16 Sep 2023* | ***Revised:*** *19 Sep 2023* | ***Accepted:*** *22 Sep 2023*